

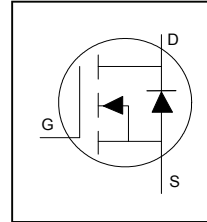
Application

- Optimized for UPS/Inverter Applications
- Low Voltage Power Tools

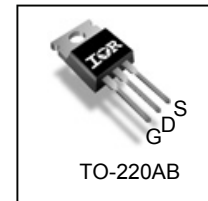
Benefits

- Best in Class Performance for UPS/Inverter Applications
- Very Low RDS(on) at 4.5V VGS
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free, RoHS Compliant

HEXFET® Power MOSFET



V_{DSS}	30	V
R_{DS(on)} max (@ V _{GS} = 10V)	3.5	mΩ
(@ V _{GS} = 4.5V)	4.5	
Q_g (typical)	36	nC
I_D (Silicon Limited)	150④	A
I_D (Package Limited)	78A	



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLB4132PbF	TO-220AB	Tube	50	IRLB4132PbF

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	30	V
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	150④	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	100	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Package Limited)	78	
I _{DM}	Pulsed Drain Current ①	620	
P _D @ T _C = 25°C	Maximum Power Dissipation ⑥	140	W
P _D @ T _C = 100°C	Maximum Power Dissipation ⑥	68	W
	Linear Derating Factor	0.90	W/°C
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N-m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ⑥	—	1.11	°C/W
R _{θCS}	Case-to-Sink, Flat Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient ⑤	—	62	

Notes ① through ⑦ are on page 8

Static @ T_J = 25°C (unless otherwise specified)

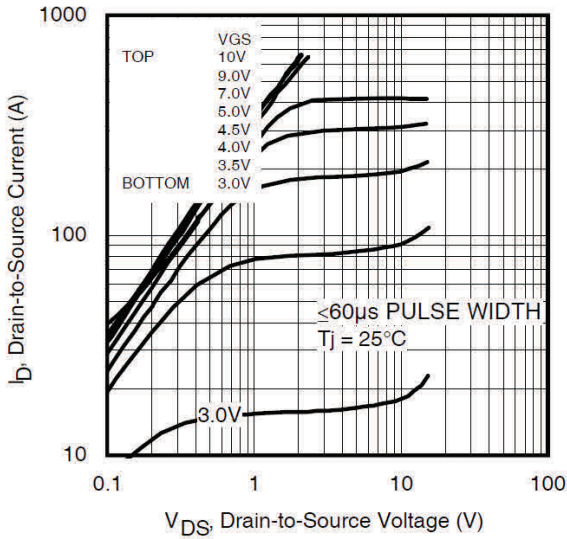
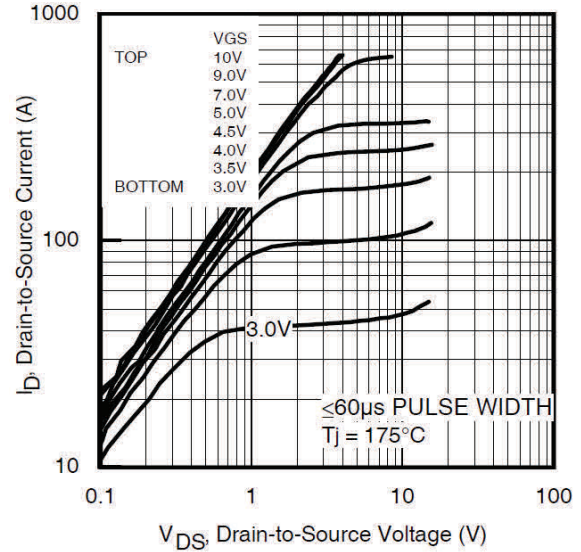
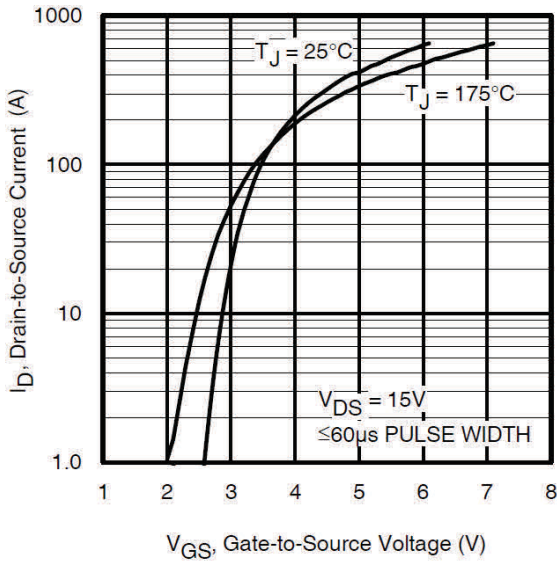
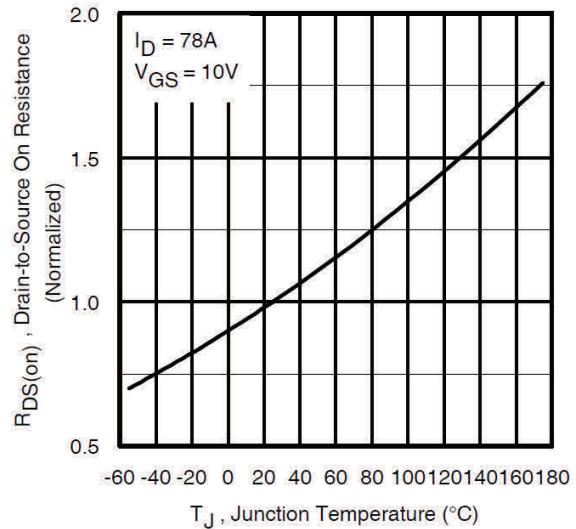
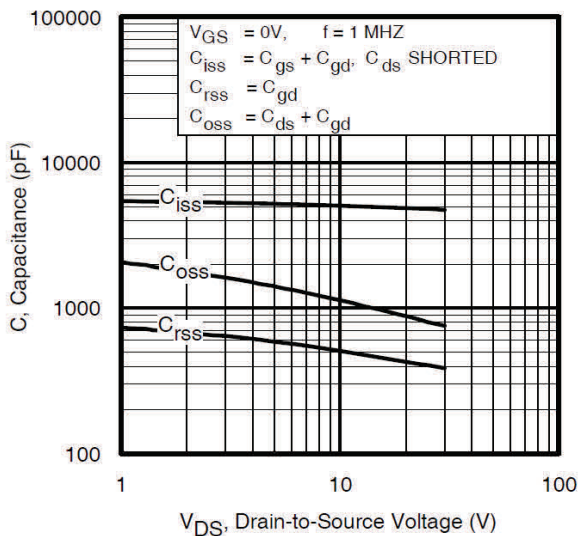
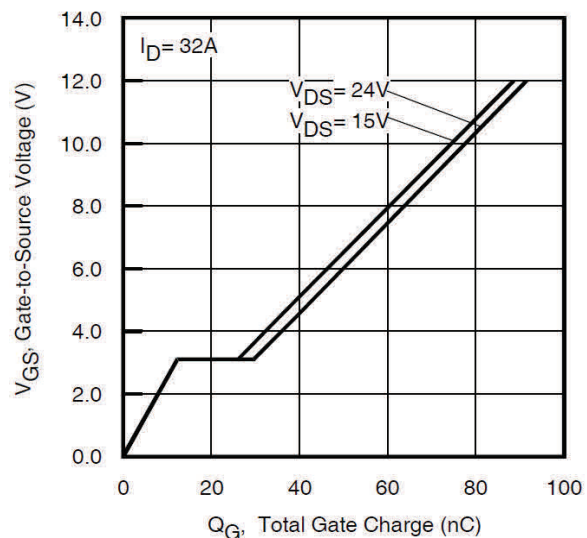
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	17	—	mV/°C	Reference to 25°C, I _D = 1mA ①
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	2.5	3.5	mΩ	V _{GS} = 10V, I _D = 40A ③
		—	3.5	4.5		V _{GS} = 4.5V, I _D = 32A ③
V _{GS(th)}	Gate Threshold Voltage	1.35	1.8	2.35	V	V _{DS} = V _{GS} , I _D = 100μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-7.7	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	100		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	190	—	—	S	V _{DS} = 15V, I _D = 32A
Q _g	Total Gate Charge	—	36	54	nC	V _{DS} = 15V V _{GS} = 4.5V I _D = 32A
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	9.1	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	4.2	—		
Q _{gd}	Gate-to-Drain Charge	—	13	—		
Q _{godr}	Gate Charge Overdrive	—	13	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	17.2	—		
Q _{oss}	Output Charge	—	21	—		
R _G	Gate Resistance	—	0.85	1.5	Ω	
t _{d(on)}	Turn-On Delay Time	—	23	—	ns	V _{DD} = 15V I _D = 32A R _G = 1.8Ω V _{GS} = 4.5V ③
t _r	Rise Time	—	92	—		
t _{d(off)}	Turn-Off Delay Time	—	25	—		
t _f	Fall Time	—	36	—		
C _{iss}	Input Capacitance	—	5110	—	pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz
C _{oss}	Output Capacitance	—	960	—		
C _{rss}	Reverse Transfer Capacitance	—	440	—		

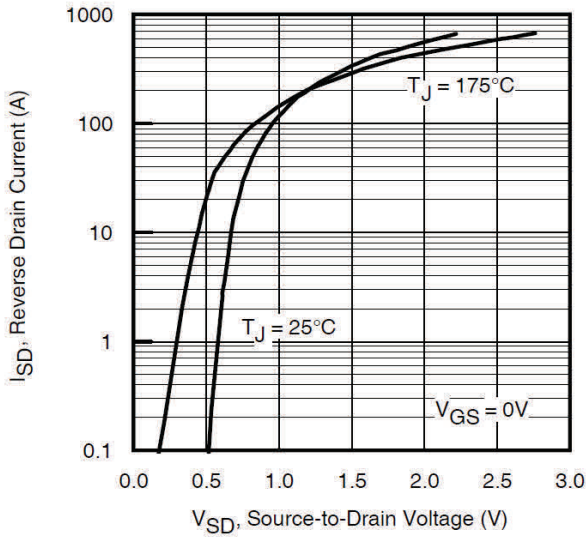
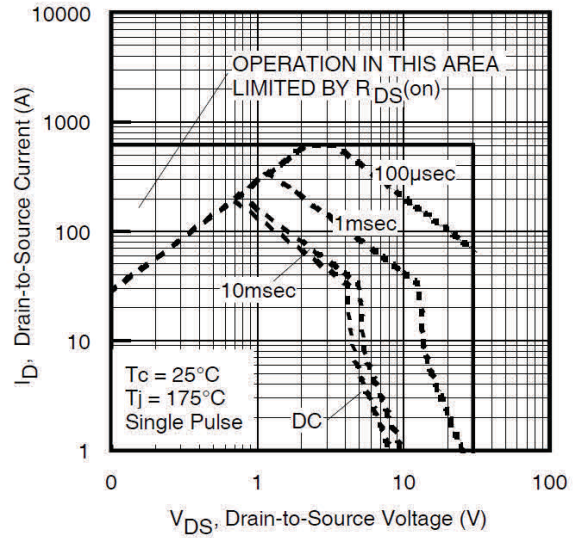
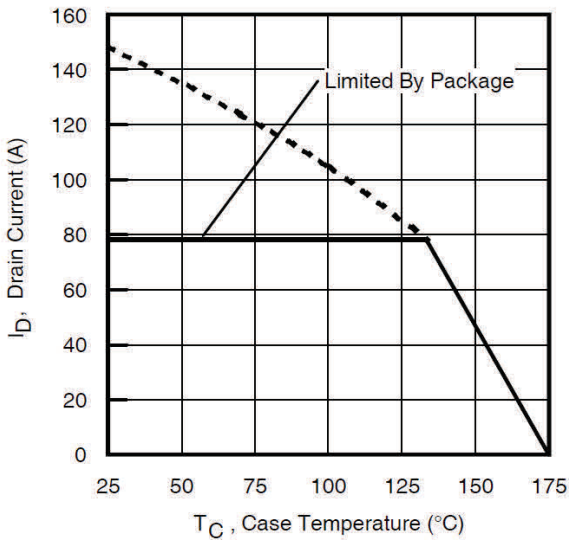
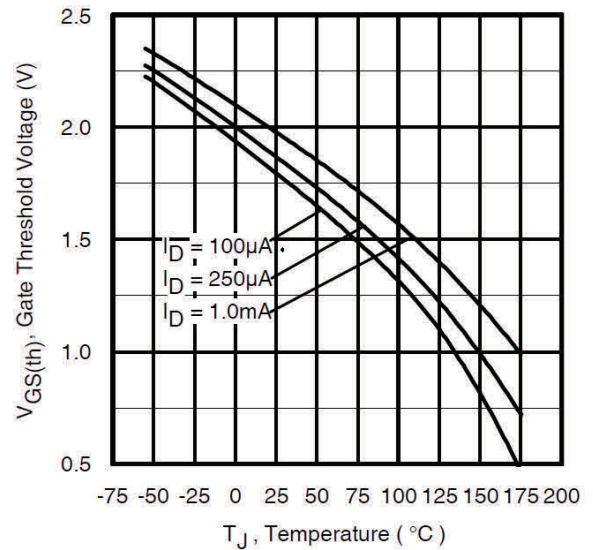
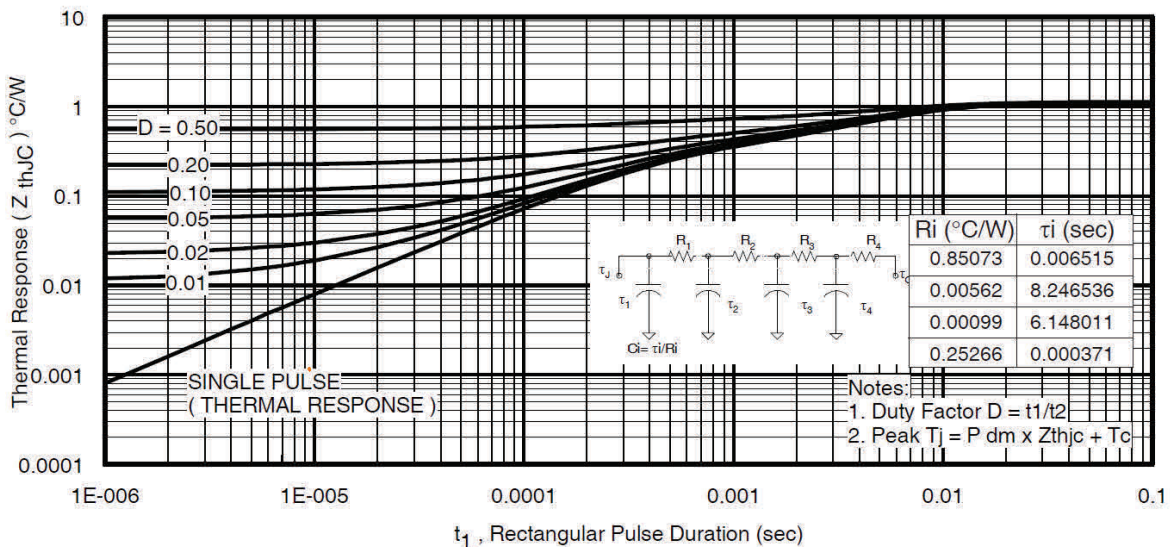
Avalanche Characteristics

E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	310	mJ
E _{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑦	900	
I _{AR}	Avalanche Current ①	32	A
E _{AR}	Repetitive Avalanche Energy ①	14	mJ

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode) ①	—	—	150 ④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	620		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 32A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	29	44	ns	T _J = 25°C I _F = 32A, V _{DD} = 15V
Q _{rr}	Reverse Recovery Charge	—	49	74	nC	di/dt = 200A/μs ③


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

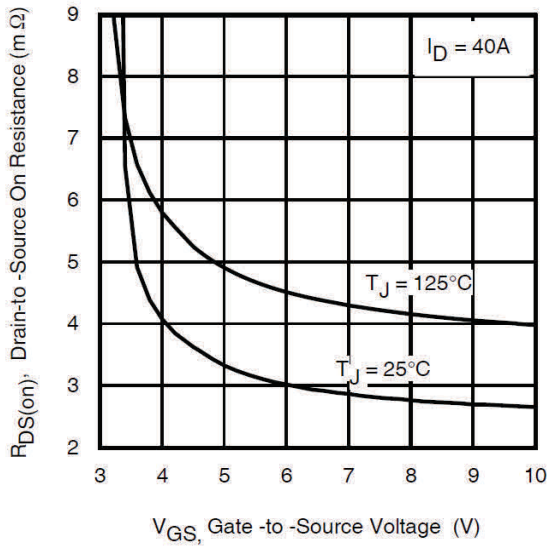


Fig 12. Typical On-Resistance vs. Gate Voltage

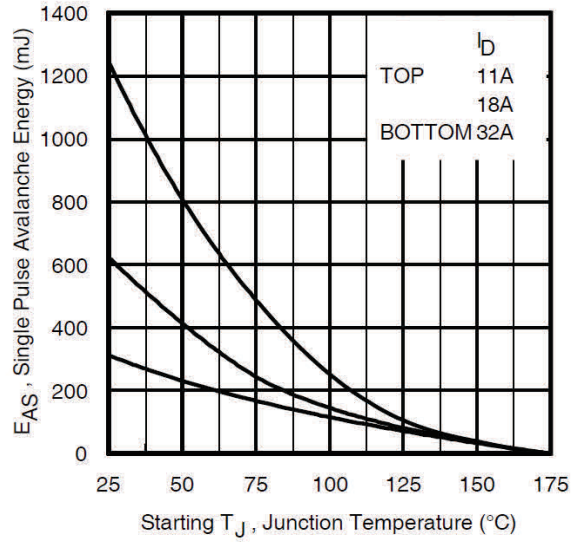


Fig 13. Maximum Avalanche Energy vs. Drain Current

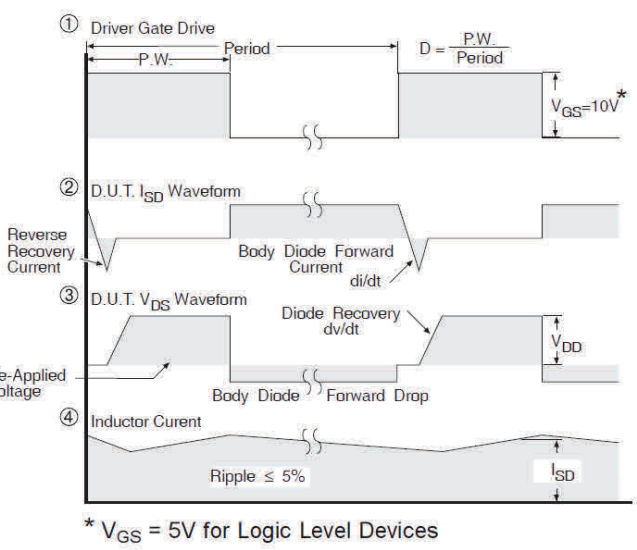
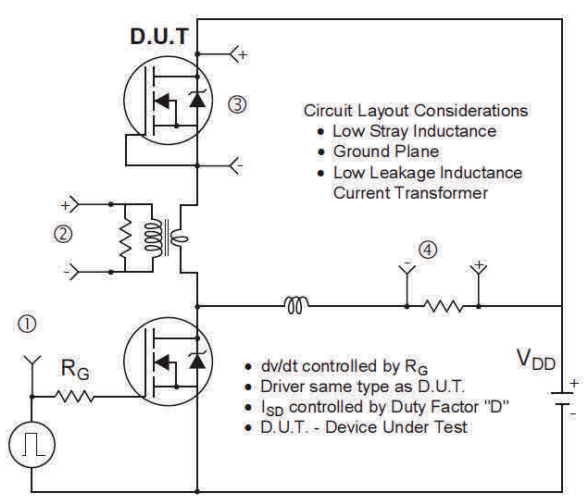


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

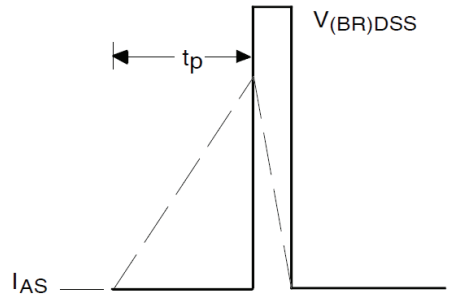
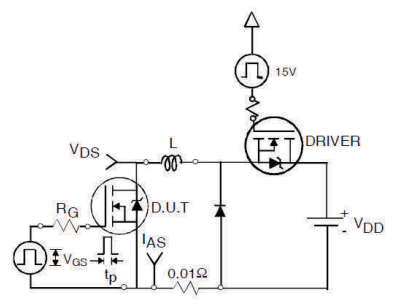


Fig 15a. Unclamped Inductive Test Circuit

Fig 15b. Unclamped Inductive Waveforms

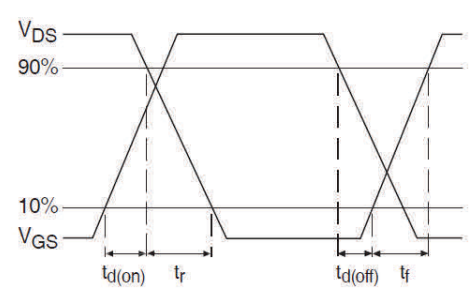
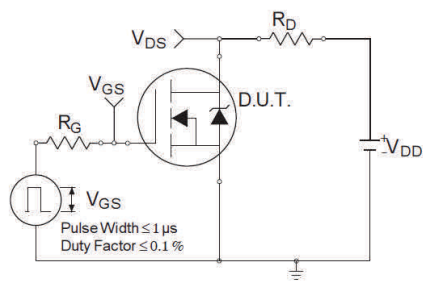


Fig 16a. Switching Time Test Circuit

Fig 16b. Switching Time Waveforms

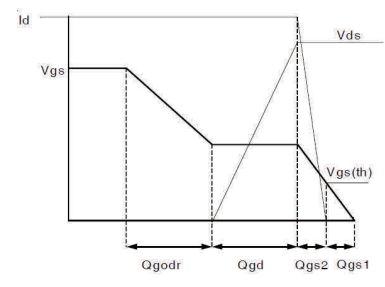
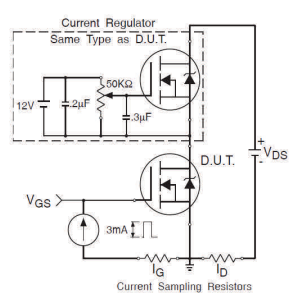
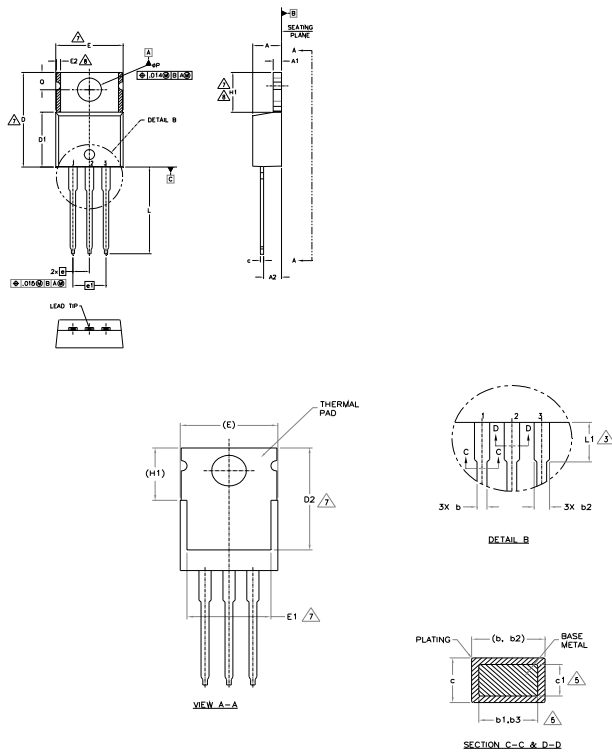


Fig 17a. Gate Charge Test Circuit

Fig 17b. Gate Charge Waveform

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

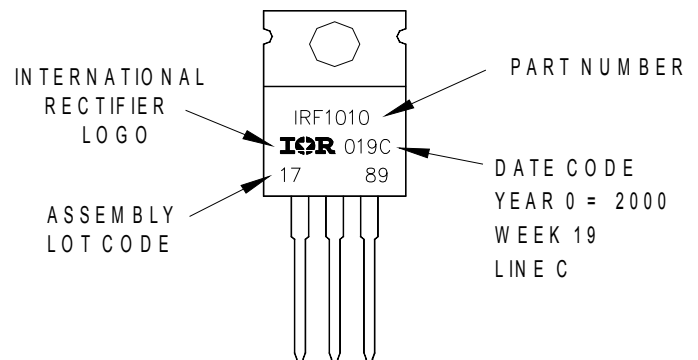
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

- LEAD ASSIGNMENTS**
- HEXFET**
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
- IGBTs, CoPACK**
- 1.- GATE
 - 2.- COLLECTOR
 - 3.- EMITTER
- DIODES**
- 1.- ANODE
 - 2.- CATHODE
 - 3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 2000
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	TO-220AB	N/A
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^{\circ}C$, $L = 0.61mH$, $R_G = 25\Omega$, $I_{AS} = 32A$.
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 78A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques Refer to application note #AN-994.
- ⑥ R_{θ} is measured at T_J approximately $90^{\circ}C$.
- ⑦ Starting $T_J = 25^{\circ}C$, $L = 0.50mH$, $R_G = 25\Omega$, $I_{AS} = 60A$, $V_{DD} = 25V$. (Statistical Limit)

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